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ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST P.A.
1401 CITRUS CENTER 255 SOUTH ORANGE AVENUE
P.O. BOX 3791
ORLANDO, FL 32802-3791

EXAMINER

CHEN, TSE W

ART UNIT

PAPER NUMBER

2116

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/010,738

Applicant(s)

ALIA ET AL.

Examiner

Tse Chen

Art Unit

2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 November 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 12-17, 19-25 and 27-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 12-17, 19-25 and 27-37 is/are rejected.
- 7) ☒ Claim(s) 18, 26 and 38 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated November 12, 2004.
2. Claims 12-38 are presented for examination. Applicant has canceled claims 1-11.
3. The rejections are respectfully maintained and reproduced infra for applicant's convenience.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 12-13, 19-20, 32-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, U.S. Patent 5677849, in view of Jain et al., U.S. Patent 6633987, hereinafter Jain.
6. In re claim 12, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-23], comprising:
 - A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries], each responsive to a respective local clock signal [clock signals 40-43] [col.2, ll.42-53; col.5, ll.65-66].
 - A system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals [col.3, l.63 -- col.4, l.34].

Art Unit: 2116

- A power control manager [central arbiter 1] connected to said circuit blocks for selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].
 - Each circuit block comprising a shutdown circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for preventing the system clock signal from functioning as the respective local clock signal [col.3, ll.5-12, ll.21-47; col.4, ll.35-53].
7. Smith did not discuss providing a shutdown acknowledgement signal to the power control manager.
8. Jain discloses a system-on-chip (SOC) [fig.3], comprising:
- A plurality of circuit blocks [CPU 302, RDRAM 350, ICH 340, AGP 330, MCH 310], each responsive to a respective local clock signal [fig.3; col.4, ll.45-65; col.5, ll.1-9].
 - A system clock [clock synthesizer 304] connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals [col.4, ll.50-52; col.5, ll.1-9].
 - A power control manager [inherently, some power control manager in the broadest interpretation is needed to generate C0-3 states signals to control power] connected to said circuit blocks for selectively providing a shutdown signal thereto [col.3, ll.1-6; col.4, ll.59-65; col.5, ll.18-21].
 - A shutdown circuit [inherently, some shutdown circuit in the broadest interpretation is needed in state C3] for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgement signal to said power control manager [col.3, ll.1-

Art Unit: 2116

6; col.6, ll.6-23; CPU block comprises a more specialized apparatus to perform acknowledgement and associated method steps].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith to include the shutdown acknowledgement signal taught by Jain, in order to obtain the SOC of claim 12, comprising a circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgement signal to a power control manager. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for selectively clocking the functional blocks to lower power consumption [Smith: col.1, l.15 -- col.2, l.9].

10. As to claim 13, Smith discloses that each shutdown circuit comprises a clock separation circuit [NAND 44-47] connected to the power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

11. As to claim 19, Jain discloses another system clock [ck 306 or drcg 308] connected to selected circuit blocks for providing a system clock signal thereto [clock synthesizer 304 comprises two system clocks of ck 306 and drcg 308].

In re claim 20, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries].

Art Unit: 2116

- A system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto [col.3, l.63 -- col.4, l.34].
- A power control manager [central arbiter 1] connected to said circuit blocks for selectively providing a shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].
- Each circuit block comprising:
 - A block logic circuit [NAND 44-47 and flip flops 23-26] having an input [NAND 44-47] for receiving the shutdown signal [fig.1].
 - A shutdown circuit [NAND 27-30 and inverters 36-39] connected to said block logic circuit for preventing the system clock signal from functioning as a local clock signal [col.3, ll.5-12, ll.21-47; col.4, ll.35-53].

12. Smith did not discuss providing a shutdown acknowledgement signal to the power control manager.

13. Jain discloses a system-on-chip (SOC) [fig.3], comprising:

- A plurality of circuit blocks [CPU 302, RDRAM 350, ICH 340, AGP 330, MCH 310], each responsive to a respective local clock signal [fig.3; col.4, ll.45-65; col.5, ll.1-9].
- A system clock [clock synthesizer 304] connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals [col.4, ll.50-52; col.5, ll.1-9].
- A power control manager [inherently, some power control manager in the broadest interpretation is needed to generate C0-3 states signals to control power] connected to

Art Unit: 2116

said circuit blocks for selectively providing a shutdown signal thereto [col.3, ll.1-6; col.4, ll.59-65; col.5, ll.18-21].

- Each circuit block comprising a block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed for the circuit blocks to perform some function] having an input for receiving the shutdown signal [inherently, some input in the broadest interpretation is needed in order for the circuit block to transition to C3], and an output for providing a shutdown acknowledgement signal to said power control manager [inherently, an output in the broadest interpretation is needed in order for the acknowledgement signal to the C3 transition to be known] after receiving the shutdown signal [col.3, ll.1-6; col.6, ll.6-23; CPU block comprises a more specialized apparatus to perform acknowledgement and associated method steps].
- A shutdown circuit [inherently, some shutdown circuit in the broadest interpretation is needed in state C3] for preventing the system clock signal from functioning as a local clock signal after the block logic circuit provides the shutdown acknowledgement signal to said power control manager [col.3, ll.1-6; col.6, ll.6-23; CPU block comprises a more specialized apparatus to perform acknowledgement and associated method steps].

14. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith to include the shutdown acknowledgement signal taught by Jain, in order to obtain the SOC of claim 20, comprising a circuit block comprising a block logic circuit having an input for receiving the shutdown signal, and an output for providing a shutdown acknowledgement signal to said power control manager after receiving the shutdown signal and a shutdown circuit

Art Unit: 2116

connected to said block logic circuit for preventing the system clock signal from functioning as a local clock signal after said block logic circuit provides the shutdown acknowledgement signal to said power control manger. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for selectively clocking the functional blocks to lower power consumption [Smith: col.1, 1.15 -- col.2, 1.9].

15. In re claims 32 and 33, Smith and Jain teach SOC as discussed above in reference to claims 12 and 13. Therefore, Smith and Jane teach method of operating the SOC.

16. Claims 14-16, 22-24, 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Jain as applied to claims 12 and 32 above, and further in view of Mejyr, U.S. Patent 6674821.

17. In re claim 14, Smith and Jain disclose each and every limitation of the claim as discussed above in reference to claim 12. In particular, Smith discloses the SOC wherein:

- Said power control manager is connected to each shutdown circuit through a respective power down request line [start_clock lines 15-18] for providing the shutdown signal thereto [fig.1; col.3, 11.5-12; connects through NAND 44-47].

18. Smith and Jain did not disclose expressly a power down acknowledgement line.

19. Mejyr discloses a system wherein:

- A power control manager [processor A 10] is connected to a shutdown circuit [processor B 20] through a respective power down request line [eclk_req 11] for providing the shutdown signal thereto, and through a respective power down acknowledgement line [eclk_ack 22] for receiving the shutdown acknowledgment signal therefrom [fig.1; col.3, 11.8-31; disable clock to power down].

Art Unit: 2116

20. It would have been obvious to one of ordinary skill in the art, having the teachings of Mejyr, Smith and Jain before him at the time the invention was made, to use the power down acknowledgement line as taught by Mejyr for the SOC disclosed by Smith and Jain as the power down acknowledgment line taught by Mejyr is a well known interconnection to be suitable for use in the SOC of Smith and Jain. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to communicate an acknowledgement between a sender and receiver [Mejyr: col.3, ll.8-31].

21. As to claim 15, Smith discloses the SOC wherein:

- Each circuit block further comprises a block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed to perform some function] connected to said shutdown circuit [fig.1; connected via lines 19-22].

22. Smith and Jain did not discuss other communication lines connecting the block logic circuit and shutdown circuit.

23. Mejyr discloses a circuit block [processors A 10 and B 20] that comprises:

- A block logic circuit [processor B 20] connected to a shutdown circuit [processor A 10] through a respective power down request line [eclk_req] for receiving the shutdown signal therefrom, and through the respective power down acknowledgement line [eclk_ack] for providing the shutdown acknowledgement thereto [fig.1; col.3, ll.8-31].

24. It would have been obvious to one of ordinary skill in the art, having the teachings of Mejyr, Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith and Jain to include the interconnections between the block logic and shutdown circuits taught by Mejyr, in order to obtain the SOC wherein each circuit block further comprises a block

Art Unit: 2116

logic circuit connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgement line for providing the shutdown acknowledgement signal thereto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for synchronizing clock control [Mejyr: col.1, 1.5 -- col.2, 1.37].

25. As to claim 16, Mejyr discloses a shutdown circuit [processor A 10] that comprises a logic circuit [clkctrl 100] having a first input [ctrl 2] connected to the respective power down request line, a second input [eclk_ack] connected to the respective power down acknowledgement line, and a third input [ext_clk] connected to the system clock, and an output for providing the respective local clock signal [main_clk] based upon logic states of the shutdown signal, the shutdown acknowledgement signal and the system clock signal [fig.2; col.3, 1.32 -- col.5, 1.37].

26. In re claim 22, Smith and Jain disclose each and every limitation of the claim as discussed above in reference to claim 20. In particular, Smith discloses the SOC wherein:

- Said power control manager is connected to each circuit block through a respective power down request line [start_clock lines 15-18] for providing the shutdown signal thereto [fig.1; col.3, 11.5-12; connects through NAND 44-47].

27. Smith and Jain did not disclose expressly a power down acknowledgement line.

28. Mejyr discloses a system wherein:

- A power control manager [processor A 10] is connected to a shutdown circuit [processor B 20] through a respective power down request line [eclk_req 11] for providing the shutdown signal thereto, and through a respective power down acknowledgement line

Art Unit: 2116

[eclk_ack 22] for receiving the shutdown acknowledgment signal therefrom [fig.1; col.3, ll.8-31; disable clock to power down].

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Mejyr, Smith and Jain before him at the time the invention was made, to use the power down acknowledgement line as taught by Mejyr for the SOC disclosed by Smith and Jain as the power down acknowledgment line taught by Mejyr is a well known interconnection to be suitable for use in the SOC of Smith and Jain. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to communicate an acknowledgement between a sender and receiver [Mejyr: col.3, ll.8-31].

30. As to claim 23, Smith discloses the SOC wherein:

- Each circuit block further comprises a block logic circuit [NAND 44-47 and flip flops 23-26] connected to said shutdown circuit [NAND 27-30 and inverters 36-39].

31. Smith and Jain did not discuss other communication lines connecting the block logic circuit and shutdown circuit.

32. Mejyr discloses a circuit block [processors A 10 and B 20] that comprises:

- A block logic circuit [processor B 20] connected to a shutdown circuit [processor A 10] through a respective power down request line [eclk_req] for receiving the shutdown signal therefrom, and through the respective power down acknowledgement line [eclk_ack] for providing the shutdown acknowledgement thereto [fig.1; col.3, ll.8-31].

33. It would have been obvious to one of ordinary skill in the art, having the teachings of Mejyr, Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith and Jain to include the interconnections between the block logic and shutdown circuits

Art Unit: 2116

taught by Mejyr, in order to obtain the SOC wherein each circuit block further comprises a block logic circuit connected to said shutdown circuit through the respective power down request line for receiving the shutdown signal therefrom, and through the respective power down acknowledgement line for providing the shutdown acknowledgement signal thereto. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for synchronizing clock control [Mejyr: col.1, l.5 -- col.2, l.37].

34. As to claim 24, Mejyr discloses a shutdown circuit [processor A 10] that comprises a logic circuit [clkctrl 100] having a first input [ctrl 2] connected to the respective power down request line, a second input [eclk_ack] connected to the respective power down acknowledgment line, and a third input [ext_clk] connected to the system clock, and an output for providing the respective local clock signal [main_clk] based upon logic states of the shutdown signal, the shutdown acknowledgement signal and the system clock signal [fig.2; col.3, l.32 -- col.5, l.37].

35. As to claims 34-36, Mejyr, Smith and Jain teach SOC as discussed above in reference to claims 14-16. Therefore, Smith and Jane teach method of operating the SOC.

36. Claims 17, 25, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mejyr, Smith, and Jain as applied to claims 14 and 34 above, and further in view of Mohammad, U.S. Patent 6675305.

37. In re claim 17, Mejyr, Smith, and Jain disclose each and every limitation of the claim as discussed above in reference to claim 14. In particular, Mejyr discloses the power control manager [processor A 10] that comprises:

Art Unit: 2116

- A first register [clock control register] connected to the respective power down request lines for storing data indicating logic states of the shutdown signal [ctrl 2] [col.4, ll.28-35].
38. Mejyr, Smith, and Jain did not discuss a second register.
39. Mohammad discloses a system [100] comprising:
- A first register [control register 114] connected to the respective request lines [inherently, some kind of lines are needed to propagate the request signal to the register] for storing data [parameters] indicating logic states of the request signals [col.3, ll.29-32; parameters indicate the requested functionality to be performed].
 - A second register [status register 115] connected to the respective power down acknowledgement lines [inherently, some kind of lines are needed to propagate the acknowledgement signal to the register] for storing data [event] indicating logic states of the acknowledgement signals [col.3, ll.33-35; events occur as acknowledgements to performed functions].
40. It would have been obvious to one of ordinary skill in the art, having the teachings of Mohammad, Mejyr, Smith and Jain before him at the time the invention was made, to modify the SOC taught by Mejyr, Smith and Jain to include the dual buffers taught by Mohammad, in order to obtain the SOC wherein the power control manager comprises a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals and a second register connected tot the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals. One of ordinary

Art Unit: 2116

skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption with clock control [Mohammad: col.1, ll.39-54].

41. In re claim 25, Mejyr, Smith, and Jain disclose each and every limitation of the claim as discussed above in reference to claim 22. In particular, Mejyr discloses the power control manager [processor A 10] that comprises:

- A first register [clock control register] connected to the respective power down request lines for storing data indicating logic states of the shutdown signal [ctrl 2] [col.4, ll.28-35].

42. Mejyr, Smith, and Jain did not discuss a second register.

43. Mohammad discloses a system [100] comprising:

- A first register [control register 114] connected to the respective request lines [inherently, some kind of lines are needed to propagate the request signal to the register] for storing data [parameters] indicating logic states of the request signals [col.3, ll.29-32; parameters indicate the requested functionality to be performed].
- A second register [status register 115] connected to the respective power down acknowledgement lines [inherently, some kind of lines are needed to propagate the acknowledgement signal to the register] for storing data [event] indicating logic states of the acknowledgement signals [col.3, ll.33-35; events occur as acknowledgements to performed functions].

44. It would have been obvious to one of ordinary skill in the art, having the teachings of Mohammad, Mejyr, Smith and Jain before him at the time the invention was made, to modify the SOC taught by Mejyr, Smith and Jain to include the dual buffers taught by Mohammad, in order

Art Unit: 2116

to obtain the SOC wherein the power control manager comprises a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals and a second register connected to the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption with clock control [Mohammad: col.1, ll.39-54].

45. As to claim 37, Mohammad, Mejjr, Smith and Jain teach SOC as discussed above in reference to claim 17. Therefore, Smith and Jane teach method of operating the SOC.

46. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith and Jain as applied to claim 20 above, and further in view of Jung et al., U.S. Patent 5768213, hereinafter Jung.

47. In re claim 21, Smith and Jain disclose each and every limitation of the claim as discussed above in reference to claim 20. In particular, Smith discloses that each block logic circuit comprises a clock separation circuit [NAND 44-47] connected to the power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

48. Smith and Jain did not discuss a power down request line connecting the power control manager and the shutdown circuit.

49. Jung discloses a SOC [semiconductory memory device], wherein:

- A shutdown circuit [clock generator 12] comprises a clock separation circuit [clock generator 12] connected to a power control manager [control signal generator 22] for

Art Unit: 2116

preventing the system clock signal [clk] from functioning as the local clock signal [clk 14].

50. It would have been obvious to one of ordinary skill in the art, having the teachings of Jung, Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith and Jain to include the extra connection between the power control manager and the shutdown circuit taught by Jung, in order to obtain the SOC of claim 21, comprising a shutdown circuit that comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for selectively clocking the functional blocks to lower power consumption [Smith: col.1, l.15 -- col.2, l.9].

51. Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in view of Jain, Mejyr, and Matoba.

52. In re claim 27, Smith discloses a system-on-chip (SOC) [integrated circuit] [col.1, ll.17-23], comprising:

- A plurality of circuit blocks [fig.1; function blocks 11-14 with associated logic circuitries].
- A system clock [clk_in 35] connected to said circuit blocks for providing a system clock signal thereto [col.3, l.63 -- col.4, l.34].
- A power control manager [central arbiter 1] connected to said circuit blocks through a respective power down request line [start_clock lines 15-18] for selectively providing a

Art Unit: 2116

shutdown signal [start_clock 15-18] thereto [col.2, l.53 -- col.3, l.4; start_clock is set high to shut down].

- Each circuit block comprising a shutdown circuit [NAND gates 27-30, 44-47, flip flops 23-26, inverters 36-39] for preventing the system clock signal from functioning as the respective local clock signal [col.3, ll.5-12, ll.21-47; col.4, ll.35-53].

53. Smith did not discuss details of a shutdown acknowledgement signal or a register.

54. In regards to the shutdown acknowledgement signal, Jain discloses a system-on-chip (SOC) [fig.3], comprising:

- A plurality of circuit blocks [CPU 302, RDRAM 350, ICH 340, AGP 330, MCH 310], each responsive to a respective local clock signal [fig.3; col.4, ll.45-65; col.5, ll.1-9].
- A system clock [clock synthesizer 304] connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals [col.4, ll.50-52; col.5, ll.1-9].
- A power control manager [inherently, some power control manager in the broadest interpretation is needed to generate C0-3 states signals to control power] connected to said circuit blocks for selectively providing a shutdown signal thereto [col.3, ll.1-6; col.4, ll.59-65; col.5, ll.18-21].
- Each circuit block comprising a block logic circuit [inherently, some block logic circuit in the broadest interpretation is needed for the circuit blocks to perform some function] having an input for receiving the shutdown signal [inherently, some input in the broadest interpretation is needed in order for the circuit block to transition to C3], and an output for providing a shutdown acknowledgement signal to said power control manager

Art Unit: 2116

[inherently, an output in the broadest interpretation is needed in order for the acknowledgement signal to the C3 transition to be known] after receiving the shutdown signal [col.3, ll.1-6; col.6, ll.6-23; CPU block comprises a more specialized apparatus to perform acknowledgement and associated method steps].

- A shutdown circuit [inherently, some shutdown circuit in the broadest interpretation is needed in state C3] for preventing the system clock signal from functioning as a local clock signal after the block logic circuit provides the shutdown acknowledgement signal to said power control manager [col.3, ll.1-6; col.6, ll.6-23; CPU block comprises a more specialized apparatus to perform acknowledgement and associated method steps].

55. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith to include the shutdown acknowledgement signal taught by Jain, in order to obtain the SOC of claim 27, comprising a circuit block comprising a block logic circuit having an input for receiving the shutdown signal, and an output for providing a shutdown acknowledgement signal to said power control manager after receiving the shutdown signal and a shutdown circuit connected to said block logic circuit for preventing the system clock signal from functioning as a local clock signal after said block logic circuit provides the shutdown acknowledgement signal to said power control manger. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for selectively clocking the functional blocks to lower power consumption [Smith: col.1, l.15 -- col.2, l.9].

56. Furthermore, Mejyr discloses a system wherein:

Art Unit: 2116

- A power control manager [processor A 10] is connected to a shutdown circuit [processor B 20] through a respective power down request line [eclk_req 11] for providing the shutdown signal thereto, and through a respective power down acknowledgement line [eclk_ack 22] for receiving the shutdown acknowledgment signal therefrom [fig.1; col.3, ll.8-31; disable clock to power down].

57. It would have been obvious to one of ordinary skill in the art, having the teachings of Mejyr, Smith and Jain before him at the time the invention was made, to use the power down acknowledgement line as taught by Mejyr for the SOC disclosed by Smith and Jain as the power down acknowledgment line taught by Mejyr is a well known interconnection to be suitable for use in the SOC of Smith and Jain. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to communicate an acknowledgement between a sender and receiver [Mejyr: col.3, ll.8-31].

58. In regards to the register, Matoba discloses a system comprising:

- A power control manager [system controller 15] comprising at least one register [16a] for storing data indicating logic states of the shutdown signals and the shutdown acknowledgement signals [col.8, ll.3-11, ll.48-53].
- A central processing unit [CPU #0] connected to the power control manager [fig.1] for determining whether each circuit block is in an active state or an idle state by querying the at least one register [col.8, ll.3-11; completion of a process].

59. It would have been obvious to one of ordinary skill in the art, having the teachings of Smith, Jain, Mejyr, and Matoba before him at the time the invention was made, to modify the SOC taught by Smith, Mejyr and Jain to include the register and CPU taught by Matoba, in order

Art Unit: 2116

to obtain the SOC of claim 27, comprising a power control manager comprising at least one register for storing data indicating logic states of the shutdown signals and the shutdown acknowledgement signals and a central processing unit connected to said power control manager for determining whether each circuit block is in an active state or an idle state by querying said at least one register. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for controlling power consumption amongst multiple functional blocks through various detecting means [Matoba: col.1, l.60 -- col.2, l.52].

60. As to claim 28, Smith discloses that each shutdown circuit comprises a clock separation circuit [NAND 44-47] connected to the power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state [fig.1; col.3, ll.5-12; high kill_clock is idle].

61. As to claim 29, Mejyr discloses a circuit block [processors A 10 and B 20] that comprises a block logic circuit [processor B 20] connected to a shutdown circuit [processor A 10] through a respective power down request line [eclk_req] for receiving the shutdown signal therefrom, and through the respective power down acknowledgement line [eclk_ack] for providing the shutdown acknowledgement thereto [fig.1; col.3, ll.8-31].

62. As to claim 30, Mejyr discloses a clock separation circuit [processor A 10] that comprises a logic circuit [clkctrl 100] having a first input [ctrl 2] connected to the respective power down request line, a second input [eclk_ack] connected to the respective power down acknowledgment line, and a third input [ext_clk] connected to the system clock, and an output for providing the respective local clock signal [main_clk] based upon logic states of the shutdown signal, the shutdown acknowledgement signal and the system clock signal [fig.2; col.3, l.32 -- col.5, l.37].

Art Unit: 2116

63. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Smith, Jain, Mejyr, and Matoba as applied to claim 27 above, and further in view of Mohammad.

64. In re claim 31, Matoba, Mejyr, Smith, and Jain disclose each and every limitation of the claim as discussed above in reference to claim 27. In particular, Mejyr discloses the power control manager [processor A 10] that comprises:

- A first register [clock control register] connected to the respective power down request lines for storing data indicating logic states of the shutdown signal [ctrl 2] [col.4, ll.28-35].

65. Matoba, Mejyr, Smith, and Jain did not discuss a second register.

66. Mohammad discloses a system [100] comprising:

- A first register [control register 114] connected to the respective request lines [inherently, some kind of lines are needed to propagate the request signal to the register] for storing data [parameters] indicating logic states of the request signals [col.3, ll.29-32; parameters indicate the requested functionality to be performed].
- A second register [status register 115] connected to the respective power down acknowledgement lines [inherently, some kind of lines are needed to propagate the acknowledgement signal to the register] for storing data [event] indicating logic states of the acknowledgement signals [col.3, ll.33-35; events occur as acknowledgements to performed functions].

67. It would have been obvious to one of ordinary skill in the art, having the teachings of Mohammad, Matoba, Mejyr, Smith and Jain before him at the time the invention was made, to modify the SOC taught by Mejyr, Matoba, Smith and Jain to include the dual buffers taught by

Art Unit: 2116

Mohammad, in order to obtain the SOC wherein the power control manager comprises a first register connected to the respective power down request lines for storing data indicating logic states of the shutdown signals and a second register connected tot the respective power down acknowledgment lines for storing data indicating logic states of the shutdown acknowledgment signals. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption with clock control [Mohammad: col.1, ll.39-54].

Allowable Subject Matter

68. Claims 18, 26, 38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

69. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the references, either alone or in combination discloses or renders obvious a system on chip of claims 18 and 26 or a method of claim 38, with all the limitations as stipulated in claims 18, 26, and 38 and associated base and intervening claims.

Response to Arguments

70. All rejections of claim limitations as filed prior to Amendment dated November 12, 2004 not argued in entirety or substantively in response filed as said Amendment have been conceded by Applicant and the rejections are maintained from henceforth.

71. Applicant's arguments, with respect to claim 12, have been fully considered but they are not persuasive.

Art Unit: 2116

72. Applicant alleges that Jain “fails to clearly state that each circuit block comprises a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgement signal to the power control manager.” Applicant supports this allegation with a *conclusion* that “the shutdown acknowledgement signal is also broadcast instead of being issued by the respective circuit blocks”. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In the instant case, Applicant attacked Jain individually when the rejection was based on a combination of Smith and Jain. Examiner specifically asserted in part 5 of the previous Office Action that Smith “did not discuss providing a shutdown acknowledgement signal to the power control manager” [i.e., Smith taught every limitation of the claim except the shutdown acknowledgement signal which was addressed by Jain]. As cited in part 7 of the previous Office Action and conceded by Applicant, it would have been obvious to one of ordinary skill in the art, having the teachings of Smith and Jain before him at the time the invention was made, to modify the SOC taught by Smith to include the shutdown acknowledgement signal taught by Jain, in order to obtain the SOC of claim 12, comprising a circuit block comprising a shutdown circuit for preventing the system clock signal from functioning as the respective local clock signal after the circuit block receiving the shutdown signal provides a shutdown acknowledgement signal to a power control manager. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way for selectively clocking the functional blocks to lower

Art Unit: 2116

power consumption [Smith: col.1, 1.15 -- col.2, 1.9]. Therefore, Applicant's conclusory remarks regarding Jain's shutdown and acknowledgement signal supposedly being broadcasted is not particularly relevant in the instant case.

73. As demonstrated above, Applicant's arguments, with respect to claim 12, are not persuasive and the rejection is respectfully maintained.

74. All other claims were not argued separately.

Conclusion

75. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

Art Unit: 2116

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
January 16, 2005


LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100